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10/675,744	09/30/2003	John Steven Dodson	AUS920020534US1	5989

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EXAMINER	
DARE, RYAN A	
ART UNIT	**PAPER NUMBER**
2186	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/27/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/675,744	DODSON ET AL.	
	Examiner	Art Unit	
	Ryan Dare	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 November 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☒ Claim(s) ~~*11 and 17*~~ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. The amendments to the claims made on 11/29/06 overcome the corresponding objections.

2. The amendments to the claims raise a new objection to claim 11. The second to last limitation recites "means for the first device to issue an particular address operation." The examiner believes this should be "means for the firs device to issue a particular address operation." Appropriate correction is required.

3. The amendments to the claims raise a new objection to claim 17. The fifth line recites: "is response." The Examiner believes this should be "in response." Appropriate correction is required.

Specification

4. The amendments to the specification made on 11/29/06 overcome the corresponding objections.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the

applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1-2, 7, 9 and 20 are rejected under 35 U.S.C. 102(e) as being anticipated by Arimilli et al., US Patent Application Publication 2003/0097529, hereafter Arimilli '29.

The applied reference has a common inventor and assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

7. With respect to claim 1, Arimilli '29 teaches a data processing system having a coherent memory hierarchy that includes a memory and a plurality of caches each assigned to particular ones of a plurality of devices that generate cache access operations, a method of maintaining cache coherency comprising:

when a first device issues a particular address operation, which operation requests sole ownership of a cache line and indicates that said first device has sole ownership of the cache line AND may or may not overwrite the cache line, wherein said particular address operation further causes a second device that has a most coherent copy of the cache line to not issue the most coherent copy of the cache line on the system bus, in par.18 where it describes the DClaim operation: "The DClaim operation accordingly is an address-only operation since the value does not need to be read

(From system memory or any intervening cache). Because of this attribute, the DClaim operation is more efficient than the RWITM operation, which would force the read operation across the system bus."

in response to snooping said particular address operation, changing a coherency state of the cache line in a second cache associated with a snooping device to a second state without sending data from said cache line in the second cache to the first cache, wherein a default response to a snoop of a different-type address operation requesting the cache line automatically triggers a return of the cache line from the second cache when the second cache has the most coherent copy of the cache line, in par. 81, which describes a snooping cache which transitions to the Z1 state when the above-mentioned DClaim is issued. Also refer back to par. 18, and the justification above, which describes the RWITM operation, which is the "default response" that forces a read.

wherein sole ownership of said cache line is provided to said first device without data being sourced to said first cache from another cache, in par. 18.

8. With respect to claim 2, Arimilli '29 teaches the method of Claim 1, wherein, when said first device subsequently initiates a write of said cache line, said method further comprises changing said first state to a third state indicating that a most coherent copy of said data exists within the cache line of the first cache, in the last 5 lines of par. 27.

9. With respect to claim 7, Arimilli '29 teaches the method of claim 2, further comprising:

snooping requests for access to said cache line at said first cache, in par. 20;

and when the cache line in the first cache is still in the first coherency state, retrying all snooped requests, wherein all subsequent requests snooped while said cache line is in the first coherency state is retried until the coherency state changes, in par. 20.

10. With respect to claim 9, Arimilli '29 teaches the method of claim 1, wherein said first device is an I/O device and said first cache is an I/O cache controlled by an I/O controller, in par. 18, said method further comprising:

issuing the address operation as a direct memory access (DMA) Claim in response to a speculative DMA write, in par. 18.

11. With respect to claim 20, Arimilli '29 teaches the caching mechanism of claim 1, wherein said first device is an I/O device and said caching mechanism includes an I/O cache controlled by an I/O controller, in par. 18, said method further comprising:

means issuing the address operation as a direct memory access (DMA) Claim in response to a speculative DMA write, in par. 18.

Claim Rejections - 35 USC § 103

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

14. Claims 3-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arimilli '29 as applied to claims 1-2 above, and further in view of Chaudhry, et al., US Patent Application Publication 2002/0199063.

15. With respect to claim 3, all other limitations of the parent claims are taught as discussed supra, but Arimilli '29 fails to teach speculatively issuing operations. Chaudhry et al. teach the method of claim 1, further comprising:

generating said particular address operation for a speculatively issued cache line overwrite operation, in the Abstract.

speculatively issuing the particular address operation for sole ownership of the cache line, in the Abstract; and

determining whether said cache line overwrite operation was correctly speculated, wherein said first coherency state is changed to another coherency state depending on whether said cache line overwrite operation was correctly speculated, in par. 142.

16. It would have been obvious to one of ordinary skill in the art, having the teachings of Arimilli and Chaudhry before him at the time the invention was made, to

modify the cache coherency protocol of Arimilli with the cache coherency protocol of Chaudhry in order to increase performance by allowing load and instructions to issue speculatively, as taught by Chaudhry in par. 11.

17. With respect to claim 4, Chaudhry et al. teach the method of claim 3, further comprising:

determining when said cache line overwrite was not correctly speculated, in the Abstract.

changing the coherency state of the cache line in the first cache from said first coherency state to an invalid state, in the Abstract; and

subsequently sourcing requests for said cache line from memory, in the Abstract.

18. It would have been obvious to one of ordinary skill in the art, having the teachings of Arimilli and Chaudhry before him at the time the invention was made, to modify the cache coherency protocol of Arimilli with the cache coherency protocol of Chaudhry in order to increase performance by allowing load and instructions to issue speculatively, as taught by Chaudhry in par. 11.

19. With respect to claim 5, Chaudhry et al. teach the method of claim 3, further comprising:

determining when the cache line overwrite operation was correctly speculated, in par. 142;

initiating a write of said cache line with data provided by said first device, in par. 142.

changing said first state to a third state indicating that a most coherent copy of said data exists within the cache line of the first cache, in par. 142.

20. It would have been obvious to one of ordinary skill in the art, having the teachings of Arimilli and Chaudhry before him at the time the invention was made, to modify the cache coherency protocol of Arimilli with the cache coherency protocol of Chaudhry in order to increase performance by allowing load and instructions to issue speculatively, as taught by Chaudhry in par. 11.

21. Claims 6 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arimilli '29 as applied to claims 1- 2 above, and further in view of Chang, US Patent Application Publication 2003/0115423.

22. With respect to claim 6, Arimilli teaches all other limitations of the parent claims as discussed supra, but fails to teach the snooping method of claim 6. Chang teaches the method of claim 2, further comprising:

snooping requests for access to said cache line at said first cache, in par, 64, lines 7-8.

when the cache line in said first cache is in the third coherency state and said first device has completed writing data to said first cache, sourcing the data from the first cache to the second cache, in par. 65, lines 22-25.

when the cache line in said first cache is in the invalid coherency state, sourcing the data from memory, in par. 68.

23. It would have been obvious to one of ordinary skill in the art, having the teachings of Arimilli '29 and Chang before him at the time the invention was made, to modify the cache coherency protocol of Arimilli with the cache coherency protocol of Chang, in order to limit main-memory accesses, which avoids bottlenecks, as taught by Chang in par. 9.

24. With respect to claim 8, Arimilli teaches all other limitations of the parent claims as discussed supra, but fails to teach the snooping method of claim 8. Chang teaches the method of claim 1, further comprising:

snooping a read request for said cache line at said first cache, in par. 64, lines 7-8

when the read request receives a null response and said cache line in the first cache is still in the first coherency state:

sourcing data for from memory in response to the read request and placing the data in a cache line of a next cache from which the read request was generated, in par. 68; and

changing said first coherency state to an invalid state in said first cache, in fig. 3, the read and invalidate column.

25. It would have been obvious to one of ordinary skill in the art, having the teachings of Arimilli '29 and Chang before him at the time the invention was made, to modify the cache coherency protocol of Arimilli with the cache coherency protocol of Chang, in order to limit main-memory accesses, which avoids bottlenecks, as taught by Chang in par. 9.

26. Claims 10 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arimilli '29 as applied to claim 1 above, in view of US Patent 5,943,684, hereafter Arimilli '84.

27. With respect to claim 10, Arimilli '29 teaches all other limitations of the claims above, but fails to teach a DCBZ Operation. Arimilli '84 teaches the method of claim 1, wherein said first device is a processor and said first cache is a processor cache controlled by a cache controller, in fig. 1, said method further comprising:

issuing the address operation in response to a data cache block zero (DCBZ) operation, in col. 7, lines 23-34.

28. It would have been obvious to one of ordinary skill in the art, having the teachings of Arimilli '84 and Arimilli '29 before him at the time the invention was made, to modify the cache coherency protocol of Arimilli '84 with the cache coherency protocol of Arimilli '29 in order to improve processing efficiency and to reduce congestion of the system bus, thereby improving performance, as taught by Arimilli '29 in par. 25.

29. With respect to claim 21, Arimilli '29 teaches all other limitations of the claims above, but fails to teach a DCBZ Operation. Arimilli '84 teaches the caching method of claim 1, wherein said first device is a processor and said caching mechanism includes a processor cache controlled by a cache controller, and further comprises means for issuing the address operation from the processor in response to a data cache block zero (DCBZ) operation, in col. 7, lines 23-34.

30. It would have been obvious to one of ordinary skill in the art, having the teachings of Arimilli '84 and Arimilli '29 before him at the time the invention was made, to modify the cache coherency protocol of Arimilli '84 with the cache coherency protocol of Arimilli '29 in order to improve processing efficiency and to reduce congestion of the system bus, thereby improving performance, as taught by Arimilli '29 in par. 25.

31. Claims 11-13, 15, 17-19 and 22-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arimilli '29 in view of Chaudhry et al.

32. With respect to claim 11, Arimilli '29 teaches:

In a data processing system having a memory hierarchy that includes a memory and a plurality of caches interconnected by a system bus and each accessible by particular ones of a plurality of devices, said caching mechanism comprising:

a first cache line of the first device having a cache line that is a less coherent copy than a corresponding cache line in a second cache of a second device, in par. 18;

a coherency tracking mechanism that supports at least a first coherency state, a second coherency state and a third coherency state, wherein:

said first coherency state indicates that said first cache has sole ownership of the cache line AND data within said first cache line may or may not be overwritten by said first device, in par. 62, the Exclusive state.

said second coherency state indicates that the data is invalid, in par. 62, the Invalid state; and

said third coherency state indicates that the data is a most coherent copy of said data, in par. 62, the modified state;

means for the first device to issue an particular address operation requesting sole access to said cache line and indicating that said first device intends to overwrite the cache line in the first cache, wherein said particular address operation further causes a second device that has a most coherent copy of the cache line to not issue the most coherent copy of the cache line on the system bus, in par. 18, the DClaim operation;

means for changing a coherency state of said cache line within said first cache to said first coherency state when a response is received on said system bus indicating that sole ownership has been granted to said first cache, in par. 81, which describes a snooping cache which transitions to the Z1 state when the above-mentioned DClaim is issued. Also refer back to par. 18, and the justification above, which describes the RWITM operation, which is the "default response" that forces a read.

Arimilli '29 fails to disclose that the first cache is provided sole ownership of the cache line pending an outcome of a speculative write operation of the first device that may update the cache line. Chaudhry teaches this in the Abstract and par. 142.

33. It would have been obvious to one of ordinary skill in the art, having the teachings of Arimilli and Chaudhry before him at the time the invention was made, to modify the cache coherency protocol of Arimilli with the cache coherency protocol of Chaudhry in order to increase performance by allowing load and instructions to issue speculatively, as taught by Chaudhry in par. 11.

34. With respect to claim 12, Arimilli '29 teaches the caching mechanism of claim 11, further comprising:

means for snooping the particular address operation, in par. 81; and

means, when the particular address operation is snooped while the cache line is in said third coherency state within a snooping device's cache and the snooping device determines the particular address operation is for access that does not overwrite the entire cache line, for:

issuing data from the snooping device's cache line on the data bus when access is granted to said first device, in par. 18; and

changing a coherency state of the snooping device's cache line to a fourth coherency state that indicates the first device's cache line has data in a coherent state that is as coherent or more coherent than said snooping device's cache line, in par. 82; and

means, when a snooped request of the particular address operation is received while the snooping device's cache line is in said third coherency state and the snooped operation is for sole ownership of the cache line that is to be completely overwritten by the first device, for changing a coherency state of the snooping device's cache line to said second state, and withholding any transfer of data to the first device's cache line, wherein data is not transferred on the system bus from a next cache containing a most coherent copy of the cache line data to the first cache of the first device when said first device indicates it intends to overwrite the cache line and wherein a default response to a snoop of a different-type address operation requesting the cache line automatically

triggers a return of the cache line from the second cache to the first cache when the second cache has the most coherent copy of the cache line, in par. 18.

35. With respect to claim 13, Arimilli '29 teaches the caching mechanism of claim 12, further comprising:

means for overwriting the data within said first device's cache line with data from the first device, wherein said overwriting the data within said first device's cache line with data from the first device, wherein said overwriting is only initiated after sole ownership has been granted and said first cache line is in said first coherency state, in the last 6 lines of par. 29; and

subsequently changing the coherency state of the first device's cache line to the third state indicating that a most coherent copy of said data exists within the first device's cache line, in the last 5 lines of par. 27.

36. With respect to claim 15, Arimilli '29 teaches the caching mechanism of claim 13, further comprising:

means for snooping requests for access to said cache line at said first cache, in system bus 157 of fig. 1B ,and described in par. 20;

means, when the first device's cache line is still in the first coherency state, for retrying all snooped requests, wherein all subsequent requests snooped while said cache line is in the first coherency state is retried until the coherency state changes, in fig. 1, system bus 157, and described in par. 20.

37. With respect to claim 17, Chaudhry et al. teach the caching mechanism of claim 11, further comprising:

means for generating said particular address operation for sole ownership of a cache line is response to a speculatively issued cache line overwrite operation by the first device, in the abstract;

means for speculatively issuing the address operation for sole ownership of the cache line, in the Abstract; and

means for determining whether said cache line overwrite operation was correctly speculated, wherein said first coherency state is changed to another coherency state depending on whether said cache line overwrite operation was correctly speculated, in par. 142.

38. With respect to claim 18, Chaudhry et al. teach the caching mechanism of claim 17, wherein when said cache line overwrite operation was not correctly speculated, said mechanism further comprises:

means changing the coherency state of the cache line in the first cache from said first coherency state to an invalid state, in the Abstract; and

means for subsequently sourcing requests for said cache line from memory, in the Abstract.

39. With respect to claim 19, all other limitations of the parent claims are taught as discussed supra. Chaudhry et al. teach the caching method of claim 17, wherein when said cache line overwrite operation was correctly speculated, said method further comprises:

means for initiating a write of said cache line with data provided by said first device, in par. 142.

means changing the coherency state of the first device's cache line from said first state to a third coherency, in par. 142.

40. With respect to claims 22-23, Applicant claims a data processing system that corresponds to the caching mechanism of claims 11-12, and is therefore rejected using similar logic.

41. Claims 14 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arimilli '29 and Chaudhry as applied to claims 11-13 above, in view of Chang.

42. With respect to claim 14, all other limitations of the parent claims are taught as discussed supra, but Arimilli fails to teach the specific snooping method of claim 14. Chang teaches the caching mechanism of claim 13, further comprising:

means for snooping requests for access to said cache line from a requesting device, in fig. 1, interconnect 108;

means, when the cache line is in the third coherency state and said first device has completed writing data to said cache line, for sourcing the data from the cache line to the requesting device, in fig. 1, interconnect 108 which connects all the devices;

means, when the cache line is in the second coherency state, for indicating that said data should be sourced from memory, in par. 65.

43. It would have been obvious to one of ordinary skill in the art, having the teachings of Arimilli '29, Chaudhry and Chang before him at the time the invention was made, to modify the cache coherency protocol of Arimilli and Chaudhry with the cache

coherency protocol of Chang, in order to limit main-memory accesses, which avoids bottlenecks, as taught by Chang in par. 9.

44. With respect to claim 16, all other limitations of the parent claims are taught as discussed supra, but Arimilli fails to teach the specific snooping method of claim 16. Chang teaches the caching mechanism of claim 13, further comprising:

means for snooping a read request for said cache line at said first cache, fig. 1, interconnect 108 and described in par. 64, lines 7-8

means, when the read request receives a null response and said cache line in the first cache is still in the first coherency state, for:

indicating that data for the cache line should be sourced from memory, in fig. 1 and described in par. 68; and

changing said first coherency state to an invalid state in said first cache, in fig. 3, the read and invalidate column.

45. It would have been obvious to one of ordinary skill in the art, having the teachings of Arimilli '29, Chaudhry and Chang before him at the time the invention was made, to modify the cache coherency protocol of Arimilli and Chaudhry with the cache coherency protocol of Chang, in order to limit main-memory accesses, which avoids bottlenecks, as taught by Chang in par. 9.

Response to Arguments

46. Applicant's arguments with respect to claims 1-22 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

47. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ryan Dare whose telephone number is (571)272-4069. The examiner can normally be reached on Mon-Fri 9:30-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (571)272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ryan Dare
February 20, 2007

PIERRE BATAILLE
PRIMARY EXAMINER
2/20/07